"SCIENTIST" DR. NATARAJAN SOMASUNDARAM

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Kavundampalayam, Coimbatore – 641 030
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CAREER OBJECTIVE

I aspire to pursue a highly rewarding career in both research and in academics, with challenging and healthy work environment where I can utilize my skills and knowledge efficiently for institutional growth and inspire the students to obtain leadership in my field of expertise. I believe that my technical, functional and communication skills will enable me to face the challenging career ahead.

FIELDS OF SPECIALIZATION

Reconfigurable Architectures, Embedded Computing Systems, VLSI Design, Fault-tolerant Systems, Image processing.

CURRENT DESIGNATION

Professor, Department of Electronics and Communication Engineering, Karpagam College of Engineering, Coimbatore.

EDUCATION

Post Doctoral Research 2012
College of Electronics and Information Engineering, Chosun University, Gwangju, South Korea
Bio-Inspired Reconfigurable Fault Tolerant Architecture
Investigator: Dr. Jeong-A Lee

Ph.D. 2009
College of Engineering, Anna University - Chennai, India
New Algorithms for Gray Scale Image Compression
Supevisor: Dr. Y.V. Ramana Rao

M.E. Embedded System Technologies (Gold Medalist) 2005
College of Engineering, Anna University - Chennai, India
Self-modifiable Mixed-signal SoC Architecture for Embedded Applications
Supevisor: Dr. B. Uma Maheswari

B.E. Electronics and Communication Engineering (First Class) 2002
Amrita Institute of Technology and Science, Coimbatore, India

Design and Implementation of Spironet using VLSI
Supevisor: Dr. M. Nirmala Devi

RESEARCH SUPERVISOR RECOGNITION

Anna University, Chennai (Ref.No. 1940213) 2012
Lr.No.:SUPR/19th RB/AR3, dtd.:06-August-2012 **(Old Ref.No. 19.459.03)**
Supervisor recognition for Ph.D./M.S. (By Research)

HONORS AND AWARDS

Google Faculty Research Award Nominee 2015
Nominated for Research Project titled "Design and development of Embedded Architecture for Cloud Based River Monitoring System".

Young Faculty Award 2015
Awarded by Venus International Foundation in Engineering/Electronics.

Faculty Fellowship 2014
Awarded by 27th International Conference on VLSI Design and 13th International Conference on Embedded Systems.

Research Promotion Scheme Funding 2013
Awarded by All India Council for Technical Education, Government of India, a Research Grant of Rs.22,55,000 for 3 Years.

Faculty Fellowship 2013
Awarded by 26th International Conference on VLSI Design and 12th International Conference on Embedded Systems.

Distinguished Professor 2012
Recognized by Open University Malaysia, Malaysia.

Visiting Researcher 2012
Awarded by Computer System Lab, Chosun University, South Korea.

Research Professor 2012
Selected for award by Clemson University, South Carolina, United States of America.

Post-Doctoral Fellowship 2011
Awarded by Computer System Lab, Chosun University, South Korea.

Senior Research Fellowship 2007
Awarded by Council for Scientific and Industrial Research, Government of India.

Junior Research Fellowship 2007
Selected for award by University Grants Commission, Government of India.

ISA Technovation Award Nominee 2006
Nominated for India Semiconductor Association Technovation award.

University Gold Medal 2005
Awarded by Anna University - Chennai, India for M.E. degree.

Student Fellowship 2005
Awarded by 18th International Conference on VLSI Design and 4th International Conference on Embedded Systems.

Scientist 2003
Entitled by Dr. A.P.J. Abdul Kalam.

RESEARCH AND PROFESSIONAL EXPERIENCE

Karpagam College of Engineering, Coimbatore, India 05/2015 – till date
Professor, ECE
- Taught courses for B.E. students of Electronics and Communication Engineering department and Electronics and Instrumentation Engineering department and for M.E. VLSI Design students.
- Carried out industrial consultancy works.

United Institute of Technology, Coimbatore, India 05/2014 – 05/2015
Professor & Dean – Electrical Sciences (R&D) / Head – R&D Centre
- Taught courses for B.E. students of Electronics and Communication Engineering department and for M.E. VLSI Design and M.E. Computer Science and Engineering students.
- Project Coordinator for M.E. and B.E. students.
- Carried out industrial consultancy works.

SSM College of Engineering, Komarapalayam, India 01/2013 – 04/2014
Professor, ECE / Research Committee Head
- Taught courses for B.E. students of Electronics and Communication Engineering department and for M.E. Applied Electronics students.
- Head of the Research Committee for the Institution.
- Prepared the VLSI Design Laboratory manual for B.E. students of Electronics and Communication Engineering.
- Project Coordinator for M.E. and B.E. students.
- Carried out industrial consultancy works.

Chosun University, Gwangju, South Korea 01/2012 – 04/2013
Visiting Researcher
- Extended the Scalable Error Detection Coding (SEDC) algorithm for designing self-checking ALU circuits.

SSM College of Engineering, Komarapalayam, India 03/2012 – 12/2012
Associate Professor, ECE / Research Coordinator

- Handled course on Professional Diploma in Embedded System Design in connection with MoU with OUM, Malaysia.
- Taught courses for B.E. students of Electronics and Communication Engineering department and for M.E. Applied Electronics students.
- Project Coordinator for M.E. and B.E. students.
- Carried out industrial consultancy works.

Chosun University, Gwangju, South Korea 06/2011 – 01/2012
Post Doctoral Researcher, Department of Computer Engineering / Computer Systems Lab
Investigator: Dr. Jeong-A Lee
- Invented the Scalable Error Detection Coding (SEDC) algorithm for designing self-checking reconfigurable circuits.
- Deriving inspirations from biological cells and integrating it with SEDC algorithm for experimental design of fault-tolerant reconfigurable embedded systems.

Bannari Amman Institute of Technology, Sathyamangalam, India 05/2010 – 05/2011
Assistant Professor, ECE / Professor In-charge of M.E. Embedded Systems
- Taught courses for B.E. students of Electronics and Communication Engineering department and for M.E. Embedded System students.
- Supervised M.E. and B.E. student projects.
- Established the Embedded Design Laboratory.
- Carried out industrial consultancy works.
- Department Head of Industry-Institute Partnership Cell (IIPC).
- Framed the M.E. Embedded System curriculum and syllabi.

Sri Krishna College of Engineering and Technology, Coimbatore, India 08/2009 – 04/2010
Assistant Professor, ECE / Microprocessor and Microcontroller Laboratory
- Taught courses for B.E. students of Electronics and Communication Engineering department.
- Supervised B.E. student projects.
- Developed course material for Microprocessor Architecture.
- Executed real-time projects.

Sri Krishna College of Engineering and Technology, Coimbatore, India 01/2009 – 07/2009
Senior Lecturer, ECE / Electronics Laboratory
- Taught courses for B.E. students of Electronics and Communication Engineering department.
- Supervised B.E. student projects.
- Executed real-time projects.
- Coordinated grading and labs with a team of a lecturer and a lab assistant.

College of Engineering, Anna University - Chennai, India 01/2006 – 12/2008
Ph.D. Research Scholar / Senior Research Fellowship
Supevisor: Dr. Y.V. Ramana Rao
- Developed four new gray scale image compression algorithms.
- Implemented and tested these new algorithms in FPGA.

Amrita Vishwa Vidyapeetham, Coimbatore, India 06/2005 – 12/2005
Lecturer, ECE / Project Coordinator of B.E. Electronics and Communication

- Taught courses for B.E. students of Electronics and Communication Engineering department.
- Supervised B.E. student projects.

College of Engineering, Anna University - Chennai, India 07/2003 – 05/2005
Professional Assistant, ECE / Microprocessor and Microcontroller Laboratory

- Supervised Microcontroller-based System Design Laboratory.
- Executed real-time projects.

College of Engineering, Anna University - Chennai, India 03/2002 – 06/2003
Junior Scientist
Worked with Dr. A.P.J. Abdul Kalam

- Partially modeled the BrainChip as a replacement for lost functionality in human brain.
- Partially completed the simulation of artificially-induced dreaming.
- Developed a prototype model of electronic neuron network.

PATENT

- **Error Detection Apparatus for Self-Checking Computation Processing Apparatus based on Scalable Error Detection Code, and Computation Processing System Comprising the Error Detection Apparatus**
  International Patent Application Number: PCT/KR2012/001715, filed on March 9, 2012.
  Registration No.:WO2013/133462 A1, registered on September 12, 2013.

- **Error Detection Code based Error Detection Apparatus and Self-Check Programmable Computation Unit including Error Detection Apparatus**
  International Patent Application Number: PCT/KR2012/005861, filed on July 23, 2012.
  Registration No.:WO2013/105709 A1, registered on July 18, 2013.

- **Scalable Error Detection Coding (SEDC) Generator, Self-Checking Look-up Table having the Generator and Method of Scalable Error Detection Coding**
  Korean Patent Application Number: 10-2011-0098730, filed on September 29, 2011.
  Registration No.:1012678940000, registered on May 21, 2013.

- **SEDC-based error detection apparatus for programmable boolean operation unit and self-checking programmable boolean operation unit having the apparatus**
  Korean Patent Application Number: 10-2012-0002924, filed on January 10, 2012.
  Registration No.:1012689970000, registered on May 23, 2013.

- **SEDC-based error detection apparatus for programmable shift/rotate operations unit and self-checking programmable shift/rotate operations unit having the apparatus**
  Korean Patent Application Number: 10-2012-0006065, filed on January 19, 2012.
  Registration No.:1012689980000, registered on May 23, 2013.

- **SEDC-based error detection apparatus for compare operation unit and self-checking compare operation unit having the apparatus**
  Korean Patent Application Number: 10-2012-0016622, filed on February 17, 2012.
  Registration No.:1012973180000, registered on August 9, 2013.

- **SEDC-based error detection apparatus for programmable add/subtract operations unit and self-checking programmable add/subtract operations unit having the apparatus**
  Korean Patent Application Number: 10-2012-0021150, filed on February 29, 2012.
  Registration No.:1012689960000, registered on May 23, 2013.

- **Scalable Totally Self-Checking Checker for Self-checking processing unit based on Scalable Error Detection Coding (SEDC) Algorithm and processing system having the checker**
  Korean Patent Application Number: 10-2012-0023871, filed on March 8, 2012.
  Registration No.:1012726200000, registered on June 3, 2013.

INDUSTRIAL CONSULTANCY SERVICES

Embedded Digital Camera-based Surveillance System On Going, 2014
Pursuing at United Institute of Technology, India
- Implementation of an embedded digital camera with SD card storage for use in surveillance systems.

Embedded SD/MMC Card Interface On Going, 2014
Pursuing at United Institute of Technology, India
- Implementation of an embedded interface for SD/MMC card system for use in embedded systems.

RF-based Home Appliance Control & Regulation 1 Month, 2013
M/s WeeDoo Constructions, Gobichettypalayam, India
- Implementation of an embedded RF-based transmitting unit and receiving unit for controlling and regulating home appliances.

Embedded Camera Interface 1 Month, 2013
Work done at SSM College of Engineering, India
- Implementation of an embedded interface for serial camera system for use in embedded systems.

Vehicle Tracking and Location-based Accident Mitigation System 4 Months, 2012
Work done at SSM College of Engineering, India
- Design and implementation of an embedded unit for vehicle tracking and accident mitigation with custom designed application software. The server side software is also developed.

Camera Device Driver 1 Month, 2012
Work done at SSM College of Engineering, India

- Implementation of a software driver for serial camera system for use in embedded systems.

GSM (SMS) Emulator 2 Weeks, 2012

Work done at SSM College of Engineering, India

- Implementation of a test platform for prototyping GSM-based projects. All the AT commands related to SMS is supported.

GPS Emulator 2 Weeks, 2012

Work done at SSM College of Engineering, India

- Implementation of a test platform for prototyping GPS-based projects. The real-time data generated is in NMEA format and compatible with Google Earth and Google Maps also.

Accident Mitigation System 3 Months, 2011

Work done at Bannari Amman Institute of Technology, India

- Designed a NXP ATOP Microcontroller-based accident detector and location indicator with custom designed application software.

Webcam-based English-to-Tamil Translation System 2 Months, 2011

Work done at Bannari Amman Institute of Technology, India

- Designed and developed a PC-based image processing system for recognizing specific english fonts and translating the recognized words to tamil.

Detection of Missing Balls in Spindle-type Ball Bearing 3 Months, 2010

M/s ISIRA, Chennai, India

- Designed and developed a PC-based image processing system with custom designed application.

Touch Screen-based Embedded Device Control System 2 Months, 2010

M/s V Tec Embedded and Software Solutions, Coimbatore, India

- Designed and developed an 8051 Microcontroller-based device control system using touch screen interface.

Lorry Weight Monitoring System 2 Months, 2010

M/s Giri Brothers, Chennai, India

- Designed and developed an 8051 Microcontroller, load-cell and GSM-based system for detecting the weight change in lorries and indicating via an SMS.

Autoleveller for Textile Yarn Draw-Frame Machine 6 Months, 2010

M/s Sheltronics, Coimbatore, India

- Developed an algorithm and designed a real-time signal processing system for generating the evenness deviation spectrogram.

Camera-assisted Robot Navigation System 3 Months, 2009

Work done at Sri Krishna College of Engineering and Technology, India

- Designed and developed a PC and a centralized camera-based image processing system for assisting in the navigation of a robot.

Short-Messaging Service (SMS)-based Cost Indication System 3 Months, 2009
M/s Suguna Chickens, Coimbatore, India

- Designed and developed an 8051 Microcontroller and GSM-based system for indicating the cost of poultry food to dealers, based on poultry farm data.

GPS, GSM-based College Bus Location Identification System 5 Months, 2009
Work done at Sri Krishna College of Engineering and Technology, India

- Designed and developed an 8051 Microcontroller, GPS and GSM-based system for indicating the location of college bus within the city.

Hand-held Ration Shop Smart Card Reader 1 Months, 2006
Work done at College of Engineering, Anna University - Chennai, India

- Tested and validated the proper working of the smart card reader to be implemented in ration shops by Government of Tamilnadu, India.

Beverage Vending Machine 11 Months, 2005
M/s Butterfly Enterprises, Chennai, India

- Designed and developed an 8051-based beverage vending machine consisting of 3 tasks running concurrently.

COURSES TAUGHT

Karpagam College of Engineering, India 05/2015 – till date

- ASIC Design for M.E. VLSI Design
- Embedded System Laboratory for B.E. Electronics and Instrumentation Engineering

United Institute of Technology, India 05/2014 – 05/2015

- Image Processing and Analysis for M.E. Computer Science and Engineering
- Linear Integrated Circuits for B.E. Electronics and Communication Engineering
- Signals and Systems for B.E. Electronics and Communication Engineering

SSM College of Engineering, India 03/2012 – 04/2014

- Computer Architecture and Parallel Processing for M.E. Applied Electronics
- VLSI Signal Processing for M.E. Applied Electronics
- Embedded Systems for B.E. Electronics and Communication Engineering
- VLSI Design for B.E. Electronics and Communication Engineering
- Electric Circuits and Electron Devices for B.E. Electronics and Communication Engineering

Bannari Amman Institute of Technology, India 05/2010 – 05/2011

- Embedded Real-time Systems for M.E. Embedded System
- Real-time Operating System for M.E. Embedded System
- Embedded System Design Laboratory using 8051 and FPGA for M.E. Embedded System
- RTOS Programming Laboratory using 8051 and μC/OS-II for M.E. Embedded System

- Basic VLSI Design for B.E. Electronics and Communication Engineering
- Creativity and Innovation for B.E. Electronics and Communication Engineering
- Concepts of Electronic System Design for B.E. Electronics and Communication Engineering

Sri Krishna College of Engineering and Technology, India 01/2009 – 04/2010

- Microprocessor Architecture for B.E. Electronics and Communication Engineering
- Microcontroller System Design for B.E. Electronics and Communication Engineering
- Signals and Systems for B.E. Electronics and Communication Engineering
- Digital Image Processing for B.E. Electronics and Communication Engineering
- Microprocessor and Microcontroller Laboratory for B.E. Electronics and Communication Engineering
- VLSI Design Laboratory using FPGA for B.E. Electronics and Communication Engineering

Amrita Vishwa Vidyapeetham, India 06/2005 – 12/2005

- Real-time Operating System for B.E. Electronics and Communication Engineering
- Microprocessor and Microcontroller Laboratory for B.E. Electronics and Communication Engineering

PUBLICATIONS

Journal Publications

1. V.Priyanga, V.Uma Maheswari, T.Venkatesh, S.Saravanan, P.Loganath and S.Natarajan, "Analysis of Redundant based Fault Tolerant Techniques for Embedded System", International Journal of Applied Engineering Research, Vol. 10, No. 38, pp. 28896 – 28901, May 2015.

2. K.Tamilselvan, A.Satheesh and S.Natarajan, "Real Time kernel based Hot Spot Communication using Raspberry Pi", International Journal for Scientific Research and Development, Vol. 3, No. 2, pp. 273 – 276, May 2015.

3. S. Natarajan and J.A. Lee, "Self-Checking Look-up Tables using Scalable Error Detection Coding (SEDC) Scheme", Journal of Semiconductor Technology and Science, Vol. 13, No. 5, pp. 415 – 422, October 2013.

4. S. Natarajan, J.A. Lee, F. Mehdipour, N. Ramadass and Y.V. Ramana Rao, "Scalable Error Detection Coding© (SEDC) Algorithm for Totally Self-Checking (TSC) Circuits", Consumer Electronics Times, Vol. 2, Issue 3, pp. 116 – 123, July 2013, [Special Invited Paper].

5. S. Natarajan and Y.V. Ramana Rao, "Ratio-Modified Block Truncation Coding Algorithms for Reduced Bitrates", The Imaging Science Journal, Vol. 59, No. 1, pp. 25 – 31, February 2011.

6. S. Natarajan, N. Ramadass and Y.V. Ramana Rao, “State-based Dynamic Multi-Alphabet Arithmetic Coding”, The Imaging Science Journal, Vol. 57, No. 1, pp. 30 – 36, February 2009.

7. S. Natarajan and Y.V. Ramana Rao, “Modified Log-Exp based Image Compression Algorithm”, International Journal of Computer Science and Network Security, Vol. 8, No. 9, pp. 179 – 184, September 2008.

8. N. Ramadass, S. Natarajan and J. Raja Paul Perinbam, “Dynamically Reconfigurable Embedded Architecture-An Alternative to Application-Specific Digital Signal Processing Architectures”, Journal of Computer Science, Vol. 3, No. 10, pp. 823 – 828, October 2007.

9. N. Ramadass, S. Natarajan and J. Raja Paul Perinbam, “DRESPA: An Integrated System for Reconfigurable High-speed Signal Processing Applications”, International Journal of Computer Science and Network Security, Vol. 7, No. 8, pp. 1 – 7, August 2007.

10. N. Ramadass, S. Natarajan and J. Raja Paul Perinbam, “Dynamically Reconfigurable (Self-modifiable) architecture for Embedded System-on-Chip applications”, Information Technology Journal, Vol. 6, No. 1, pp. 66 – 74, January 2007.

Conference Publications

1. S. Natarajan, Farhad Mehdipour, J.A. Lee, N.Ramadass and Y.V. Ramana Rao, “Totally Self-Checking(TSC) VLSI Circuits using Scalable Error Detection Coding (SEDC) Technique”, 5th Asian Symposium on Quality Electronic Design (asQED 2013), pp. 72 – 79, August 2013.

2. G.Revathi and S. Natarajan, “Design and Implementation of Embedded Unit for Vehicle Tracking and Automobile Accident Mitigation”, National Conference on Computer, Communication and Signal Processing (NCCCSP ‘13), pp. 49 – 52, April 2013.

3. S. Natarajan and J.A. Lee, “Scalable Error Detection Coding (SEDC) Algorithm”, US-Korea Conference on Science, Technology and Entrepreneurship (UKC2012), Poster Session, ECE-PP-19, August 2012.

4. S. Natarajan, “Bio-Inspired Reconfigurable Fault Tolerant Architecture”, progress report, 5th Workshop on Communication Systems for Next Generation (TR-COM-11-05-KSK), 9 pages, December 2011.

5. S. Natarajan, N. Ramadass, Y.V. Ramana Rao and J. Raja Paul Perinbam, “A Non-Volatile Mixed-Signal Data Storage Cell for use in Reconfigurable Mixed-Signal System on Chip”, proc. IEEE International Conference on Industrial and Information Systems (ICIIS 2006), 5 pages, August 2006.

6. N. Ramadass, S. Natarajan, S.G. Vijaya Kumari and J. Raja Paul Perinbam, “Partially Reconfigurable (Self Modifiable) architecture using 8 bit CPU in FPGA”, proc. IEEE

Internationa Conference on Industrial and Information Systems (ICIIS 2006), 5 pages, August 2006.

7. N. Ramadass, G.M.A. Ibrahim, S. Natarajan and J. Raja Paul Perinbam, "Reconfigurable architecture for Algebraic codebook search", proc. IEEE International Conference on Industrial and Information Systems (ICIIS 2006), 4 pages, August 2006.

8. S. Natarajan, N. Ramadass and Y.V. Ramana Rao, "FEMOS – A Ferroelectric MOS cell based non-volatile mixed-signal data storage for use in reconfigurable mixed-signal system-on-chip", proc. National Conference on Trends and Developments in VLSI and Embedded Systems, 3 pages, 2006.

9. N. Ramadass, G.M.A. Ibrahim, S. Natarajan and J. Raja Paul Perinbam, "A novel architecture for modified Algebraic Code book search" proc. International Conference on Mixed Design of Integrated Circuits and System (MIXDES 2006), pp. 207 – 209, June 2006.

10. S. Natarajan and N. Ramadass, "Self-Modifiable Mixed Signal SoC Architecture for Embedded Applications", proc. National Conference on Signals, Systems and Communications (NCSSC 2005), 5 pages, June 2005.

11. B. Sandhana, S. Natarajan and N. Ramadass, "'Self-modifiable' waveform generator using the PSoC Microcontroller", proc. National Conference on Signals, Systems and Communications (NCSSC 2005), 5 pages, June 2005.

12. N.Ramadass and S.Natarajan, "Energy saving in Low Power Embedded System using Dynamic Voltage Scaling Algorithm", proc. National Conference on Signals, Systems and Communications (NCSSC 2005), 4 pages, June 2005.

13. A. Muthamizh Selvan, S. Natarajan and N. Ramadass, "Reducing priority inversion problem in μC/OS RTOS using priority inheritance protocol", proc. National Conference on Signals, Systems and Communications (NCSSC 2005), 4 pages, June 2005.

14. S. Natarajan, N. Ramadass and J. Raja Paul Perinbam, "Design of an Embedded Computing System with Real-Time Operating System for prototyping of research and laboratory projects", proc. National Symposium on Nuclear Instrumentation (NSNI-2004), pp.607-610, January 2004.

15. S. Natarajan, N. Ramadass and J. Raja Paul Perinbam, "An Architecture for Real-Time Circuit Reconfiguration (RTCR)-based mixed-signal Reconfigurable Embedded device", proc. International Conference on Emerging Trends (ICET 2003), 6 pages, December 2003.

16. N. Ramadass, S. Natarajan and J. Raja Paul Perinbam, "Parallel Architecture for implementation of G.729 Codec using FPGA", proc. International Conference on Emerging Trends (ICET 2003), 5 pages, December 2003.

THESIS DETAILS

Ph.D. Thesis

Title: New Algorithms for Gray Scale Image Compression

In this thesis, following four new image compression algorithms were proposed: DWT-JPEG based hybrid algorithm, state-based dynamic arithmetic coding, ratio-modified BTC and modified Log-Exp transform based algorithm. Discrete Wavelet Transforms (DWT) – Joint Photographic Expert Group (JPEG) standard based hybrid image compression algorithm uses 1-level DWT decomposition with a procedure for choosing the wavelet coefficients based on energy from the three detail subbands. State-based dynamic multi-alphabet arithmetic coding algorithm adapts efficiently to the locally occurring symbol statistics. In Ratio-Modified Block Truncation Coding (RMBTC) the ratio of pixel average and block average is encoded. Lastly, Logarithmic-Exponential (Log-Exp) transform based image compression algorithm offering high CR compared to that of JPEG standard is proposed. These algorithms were also implemented and tested in FPGA.

M.E. (Embedded System Technologies) Thesis

Title: Self-modifiable Mixed-signal SoC Architecture for Embedded Applications

In this thesis, a coarse-grain SoC architecture has been proposed. The proposed architecture addresses on-chip adaptation and self-modification through real-time circuit modification algorithms by combining a mixed-signal dynamically reconfigurable hardware with a microcontroller. It is targeted at high-throughput and temporal constrained embedded systems.

B.E. (Electronics and Communication Engineering) Thesis

Title: Design and Implementation of Spironet using VLSI

The simulation of Spirometer, a device to calculate lung parameter for diagnosis and management of respiratory disorders, was implemented using VLSI technique. It is extremely complex to estimate the reference values of lung parameters obtained by Spirometry due to several potential source of variability ranging from individual characteristics to technical aspects. This project is concerned with the design of a Spironet, a neural network processor which implements back propagation algorithm to generate spirometric reference values providing more speed factor and accuracy in computation.

PROFESSIONAL SERVICE

- Senior Member (Life time), International Society for Research and Development (ISRD) (Membership No.: SR3140900150), since 2014.
- Member, International Association of Engineers (IAENG) (Membership No.: 114234), since 2011.
- Senior Member, International Association of Computer Science and Information Technology (IACSIT) (Membership No.: 80341860), since 2011.
- Reviewer, International Conference on Fuzzy System and Data Mining (FSDM2015), 2015.
- International Technical Program Committee Member, 3rd International Japan-Egypt Conference on Electronics, Communications and Computers (JEC-ECC 2015), 2015.
- International Technical Program Committee Member, International Workshop on

Architecture-aware Simulation and Computing (AASC 2014) as part of International Conference on High Performance Computing & Simulation, 2014.

- Editorial Board Member, American Journal of Embedded Systems and Applications (AJESA).
- Editorial Board Member, International Journal of Electronics and Computer Technology (IJECT).
- Reviewer, Journal of Advances in Electronics and Communications Engineering (JAECE).
- Reviewer, International Journal of Engineering Research and Technology (IJERT) (ID: IJERTREW918).
- Reviewer, Consumer Electronics Times (CET) Journal.
- Reviewer, International Association of Scientific Innovation and Research (IASIR).
- Reviewer, Communications of the ACM.
- Reviewer, Computer Technology and Application (CTA) Journal.
- Reviewer, Journal of Computer Science.
- Reviewer, IET Electronic Letters.

TECHNICAL SKILLS

CPU Architectures: 8051, X86, ARM, RX62, MSP430, Nios II

Cross-development Tools: Keil, RIDE, HEW, Eclipse

Real-Time Operating Systems: RTX51, KR51, μCLinux, μC/OS-II

Algorithm Development Tools: Assembly Language, C, MATLAB

SoC Architectures: PSoC, FPGA, FPAA

System Simulation Tools: Modelsim, PSoC Express, Xilinx ISE, Altera Quartus, Proteus

VLSI Development Tools: Mentor Graphics EDA, Tanner EDA, TCAD, Microwind

Communication Protocols: I2C, CAN, SPI, RS232, Ethernet

LINGUISTIC SKILLS

Tamil, Hindi, English: Fluent in reading, writing and conversing.

PERSONAL DETAILS

Homepage: www.somasundaramnatarajan.webs.com

Date of Birth: 10 – September – 1980

Nationality: Indian

Gender: Male

Marital Status: Married
